REMARKS

Applicant has carefully reviewed and considered the Final Office Action mailed on September 20, 2007, and the references cited therewith.

Claims 1, 11, 13, 14, 24, 35, 37 and 43 are amended, no claims are canceled, and no claims are added; as a result, claims 1-48 are now pending in this application.

§ 102 Rejection of the Claims

Claims 1-9, 11-12, 15-21, 24, 26-34 and 37-48 were rejected under 35 USC § 102(b) as being anticipated by Schutte (U.S. Patent No. 6,092,138).

Applicant respectfully traverses the 102 rejections as follows.

Independent claims 1, 11, 24, 37, and 43 are currently amended to clarify the clock signal link being in a non-arbitrated clock signal link. This feature is illustrated in Figure 1 of the originally-filed application by the direction of the amplifiers interfacing the clock to the multiple integrated circuit controller and integrated circuits, indicating that the clock signal link is configured such that it cannot be arbitrated, e.g., it is not possible for any of the integrated circuits to control the clock signal line. Figure 1 of the present application also labels the various interfaces to the clock signal line: for the multiple integrated circuit controller the interface is labelled "clock out," and for each of the integrated circuits the interface is labelled "clock in."

Schutte appears to describe a bus system wherein any of the alleged integrated circuits may control the clock signal, either as a master, or as a slave simultaneous with the master by delaying the rising edge of the clock signal (see Col. 8, Lines 43-47). The Schutte integrated circuits appear to arbitrate amongst themselves for control of the clock under certain circumstances. Thus, Schutte does not appear to describe a non-arbitrated clock signal line configuration.

Applicant previously amended the above-mentioned independent claims to clarify the clock signal being generated by only the multiple integrated circuit control. In the Response to Arguments portion of the Office Action mailed 9/20/2007, the Examiner points out that the Schutte paragraph beginning at Col. 8, line 37 begins with

the word "optionally" in discussing a master station allowing a slave station to control the clock signal by delaying rising edge of the clock signal. The Examiner suggests that this optional relinquishment of the clock signal is simply an alternate embodiment, with the implication that the master does not have to relinquish control of the clock, and thus describes the clock signal being generated by only the multiple integrated circuit control.

However, in addition to the slave stations being able to control the clock if the master station optionally allows it, e.g., after having won an arbitration to become the master station, Schutte also describes a traditional bus arbitration scheme. For example, beginning at Col. 5, line 49, through Col. 7, line 3, Schutte describes that any of the alleged integrated circuits may become the current master station and thus generate the clock signal. In particular, see Col. 6, lines 4-10. This is not an optional process. During the arbitration, other stations can delay clock pulses. In contrast, the present application claims the clock signal being generated by only the multiple integrated circuit control. Applicant respectfully submits therefore, that Schutte does not describe the clock signal being generated by only the multiple integrated circuit control.

Additionally, the above-mentioned independent claims 1, 11, 24, 37, and 43 are also currently amended to clarify the clock signal being a continuously timing clock signal, as illustrated in Figure 3 of the present application. Applicant respectfully submits that a flat-lined clock signal isn't a continuously timing, e.g., oscillating, clock signal, as would be understood by one having ordinary skill in the art, since no periodic timing information is communicated thereby. Applicant respectfully submits that a quiet clock bus, e.g., a flat-lined signal held at on DC potential, does not constitute a continuous clock signal as would be understood by one having ordinary skill in the art since no periodic information is communicated thereby. However, in the interest of moving this application toward issue, Applicant has clarified the clock signal being a continuously timing clock signal to distinguish over a clock that periodically goes quiet, e.g., flat-lined or steady, since no timing information is conveyed by a non-varying signal.

As set forth by Applicant previously, the Schutte reference describes a portion of SCLk in Hs-mode as shown in Figure 5, having no clock oscillations. The illustrated clock signal stops oscillating. Furthermore, Col. 5, lines 53-65 describes the start condition, prior to an arbitration for control of the bus, as a quiet state of the bus, in which the clock conductors (e.g., SCL and SCLH) are left at a steady DC power supply potential level, and thus, not continuously timing. The quiet clock state is needed to implement a bus arbitration methodology as described in the Schutte reference. Thus, the Schutte reference appears to teach away from a continuously timing clock signal.

As such, and for all the reasons set forth above, Applicant respectfully submits that each and every element and limitation of independent claims 1, 11, 24, 37, and 43, as amended, are not present in the Schutte reference. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 102 rejection of these independent claims, as well as claims 2-9, 12, 15-21, 26-34, 38-42, and 44-48 that depend therefrom.

§ 103 Rejection of the Claims

Claims 10 and 22 were rejected under 35 USC § 103(a) as being unpatentable over Schutte (U.S. Patent No. 6,092,138) in view of Kawamoto (U.S. Patent No. 6,967,744).

Claims 13-14, 25 and 35 were rejected under 35 USC § 103(a) as being unpatentable over Schutte (U.S. Patent No. 6,092,138) in view of Lattice Semiconductor Corporation, "Differential Signaling" – dated May 2001.

Claim 23 was rejected under 35 USC § 103(a) as being unpatentable over Schutte (U.S. Patent No. 6,092,138) in view of Baker et al. (U.S. Patent No. 7,168,006).

Claim 36 was rejected under 35 USC § 103(a) as being unpatentable over Schutte (U.S. Patent No. 6,092,138) in view of Oppendahl (U.S. Patent No. 5,500,861).

Applicant respectfully traverses the 103 rejections as follows.

Claims 10 and 22 depend from one of independent claims 1 and 11 respectively. For the reasons provided above with respect to the 102 rejections, Applicant respectfully

submits that independent claims 1 and 11 are allowable in view of the Schutte reference. From the Applicant's review, the Kawamoto reference does not cure the deficiencies of the Schutte reference with respect to Claims 1 and 11. That is, the Kawamoto reference does not describe, teach or suggest a non-arbitrated clock signal link, nor a continuously timing clock signal, nor a clock signal generated by only the multiple integrated circuit controller. As such, the references do not, either independently or in combination, describe, teach or suggest each and every element and limitation of independent claims 1 or 11, as amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of dependent claims 10 and 22 which depend from allowable claim 1 and 11 respectively.

Claims 13, 14, 25 and 35 depend from one of independent claims 11 and 24 respectively. For the reasons provided above with respect to the 102 rejections, Applicant respectfully submits that independent claims 11 and 24 are allowable in view of the Schutte reference. From the Applicant's review, the Lattice reference does not cure the deficiencies of the Schutte reference with respect to claims 11 and 24. That is, the Lattice reference does not describe, teach or suggest a non-arbitrated clock signal link, nor a continuously timing clock signal, nor a clock signal generated by only the multiple integrated circuit controller.

As such, the references do not, either independently or in combination, describe, teach or suggest each and every element and limitation of independent claims 11 or 24, as amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of dependent claims 13, 14, 25 and 35 which depend from allowable claims 11 and 24 respectively.

Claim 23 depends from one of independent claim 11. For the reasons provided above with respect to the 102 rejections, Applicant respectfully submits that independent claim 11 is allowable in view of the Schutte reference. From the Applicant's review, the Baker reference does not cure the deficiencies of the Schutte reference with respect to claim 11. That is, the Baker reference does not describe, teach

or suggest a non-arbitrated clock signal link, nor a continuously timing clock signal, nor a clock signal generated by only the multiple integrated circuit controller.

As such, the references do not, either independently or in combination, describe, teach or suggest each and every element and limitation of independent claim 11, as amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of dependent claim 23, which depends from allowable claim 11.

Claim 36 depends from independent claim 24. For the reasons provided above with respect to the 102 rejections, Applicant respectfully submits that independent claim 24 is allowable in view of the Schutte reference. From the Applicant's review, the Oppedahl reference does not cure the deficiencies of the Schutte reference with respect to claim 24. That is, the Oppedahl reference does not describe, teach or suggest a non-arbitrated clock signal link, nor a continuously timing clock signal, nor a clock signal generated by only the multiple integrated circuit controller. Therefore, the references do not, either independently or in combination, describe, teach or suggest each and every element and limitation of claim 36, as amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of dependent claim 36.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Robert Wasson at (360) 212-2338.

At any time during the pendency of this application, please charge any additional fees or credit overpayment to the Deposit Account No. 08-2025.

CERTIFICATE UNDER 37 CFR §1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: **MS RCE** Commissioner for Patents, P.O. BOX 1450 Alexandria, VA 22313-1450, on this 15th day of November, 2007.

Alison L. Sulendran
Name

Signature

Respectfully Submitted,
William S. Eaton

By Applicant's Representatives,
Brooks, Cameron & Huebsch, PLLC
1221 Nicollet Avenue, Suite 500
Minneapolis, MN 55403

By: _____
Edward J. Brooks III
Reg. No. 40,925

Date: 11/15/2007